# WEST Search History

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DATE: Tuesday, February 01, 2005

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| | *DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | |
| ☐ | L9 | l1 and l4 | 2 |
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| ☐ | L4 | (delay near2 driver) | 1961 |
| ☐ | L3 | bistable with (delay near2 driver) | 0 |
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| ☐ | L1 | (clock with grid with skew$4) | 28 |

END OF SEARCH HISTORY

L9: Entry 1 of 2 File: USPT Sep 28, 2004

DOCUMENT-IDENTIFIER: US 6799308 B2
TITLE: Timing analysis of latch-controlled digital circuits with detailed clock skew analysis

Brief Summary Text (12):
The clocks can become misaligned due to uncertainties associated with wire delay, clock driver size and variations in process, voltage and temperature across the integrated circuit chip. As a result, the registers may interpret time indicated by the local clock signals (.phi. and .phi.' in FIG. 3A) differently. Consider the case when the clock signal for the second register is delayed, or "skewed," as shown in FIG. 3B. The late arriving rising edge of the delayed clock .phi.' postpones the sampling of the input of the second register.

Detailed Description Text (35):
FIG. 6A shows a grid for domain 54 as an illustrative example. Any timing path having controlling clock signals that originate and terminate within block 54 can be defined as having a local skew (even though the signals may pass through other blocks between the origination and the termination). Local skew values can be determined using a single skew value, such as zero, in a timing analysis. As shown in FIG. 6A, the skew between domain 54 and domains 34, 43, 44; 45, 52, 53, 55, 56, 63, 64, 65 and 74 corresponds to regional skew. Relative to domain 54, any domain outside the local and regional areas exhibits a global skew. The skew values corresponding to each square in the grid correspond to skew values in a clock skew matrix. For example, the skew values shown in the grid correspond to values in, for example, a column of a clock skew matrix representing domain 54.

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L9: Entry 2 of 2 File: DWPI Mar 15, 2002

DERWENT-ACC-NO: 2002-605582
DERWENT-WEEK: 200265


TITLE: Equivalent circuit modeling method for analyzing clock skew of multiplex driving clock grid circuit network

Basic Abstract Text (1):
NOVELTY - An equivalent circuit modeling method is provided to accurately estimate a delay time of a multiplex driving clock grid circuit and analyze a clock skew by considering an influence of a parasitic component, and by rapidly analyzing timing, electric power and signal integrity.

Basic Abstract Text (2):
DETAILED DESCRIPTION - A two-dimensional table is automatically generated for estimating an input transition delay, a cell delay and an output transition delay using a standard parasite format file(30). An effective capacitance corresponding to each driver is estimated. An equivalent circuit of the effective capacitance is generated(32). The cell delay and the output transition delay of each driver are estimated using the two-dimensional table(34). An effective resistance of each driver is estimated. A single resistor voltage ramp model is generated as the standard parasite format file(36). A radio wave delay and a transition delay of each loading terminal of the single resistor voltage ramp model are estimated(38). An arriving time and a transition delay up to each loading terminal are estimated. A clock skew is estimated(40). The arriving time, the transition delay and the clock skew are displayed(42).

Standard Title Terms (1):
EQUIVALENT CIRCUIT METHOD CLOCK SKEW MULTIPLEX DRIVE CLOCK GRID CIRCUIT NETWORK

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